WHAT IS CLAIMED IS:

1. A method for managing an allocation of a portion of a memory associated with a central processing unit system that can be selectively coupled to a bus of the central processing unit system, comprising the steps of:

allocating a first portion of the memory for a first range of addresses;

selectively coupling the allocated first portion of the memory to the bus of the central processing unit system;

decoupling the selectively coupled first portion of the memory from the bus of the central processing unit system; and

reallocating the decoupled first portion of the memory for a second range of addresses.

2. The method of claim 1, comprising the steps of:

allocating a second portion of the memory for a third range of addresses;

selectively coupling the allocated second portion of the memory to the bus of the central processing unit system; and

decoupling the selectively coupled second portion of the memory from the bus of the central processing unit system.

3. The method of claim 1, wherein the step of allocating comprises the step of:

requesting the allocation of the first portion of the memory.

4. The method of claim 1, wherein the step of allocating comprises the step of:

determining the first range of addresses by locating available memory space in a system memory space associated with the central processing unit system.

5. The method of claim 4, wherein the step of allocating comprises the step of:

reserving the first range of addresses within the system memory space for the first portion of the memory.

6. The method of claim 5, wherein the step of allocating comprises the step of:

requesting the first portion of the memory for the system memory space at the first range of addresses.

7. The method of claim 1, wherein the step of allocating comprises the step of:

determining the availability of the first portion of the memory.

8. The method of claim 6, wherein the step of allocating comprises the step of:

assigning the first range of addresses in the system memory space to the first portion of the memory.

9. The method of claim 1, wherein the step of coupling comprises the step of:

returning a pointer to the first portion of the memory.

10. The method of claim 1, wherein the step of decoupling comprises the step of:

assigning a last address of the memory to the decoupled first portion of the memory.

11. The method of claim 10, wherein the step of decoupling comprises the step of:

appending the decoupled first portion of the memory to the memory at the last address.

12. A system for managing an allocation of a portion of a memory, comprising:

at least one central processing unit;

at least one bus connected to the at least one central processing unit; and

at least one memory module associated with a memory, wherein the at least one memory module is electrically decoupled from the at least one bus, and wherein the at least one memory module comprises:

means for electrically coupling the at least one memory module with the at least one bus, and

at least one memory unit.

13. The system of claim 12, wherein the at least one memory block comprises:

an address decoder for reconfiguring a portion of an address of the at least one memory module, and

a command interface for receiving commands for allocating the at least one memory module.

14. The system of claim 13, comprising:

a memory manager coupled with the at least one memory module and the at least one central processing unit, wherein the at least one memory module is coupled with the memory manager using the command interface, and wherein the memory manager is configured to allocate the at least one memory module for a range of addresses in a system memory space of the at least one central processing unit.

15. The system of claim 14, wherein the range of addresses in the system memory space of the at least one central processing unit is assigned for use by the at least one memory module while the memory module is decoupled from the at least one bus.

16. The system of claim 14, wherein an allocated at least one memory module is accessed using a pointer to the allocated at least one memory module when the allocated at least one memory module is coupled to the bus.

17. The system of claim 12, wherein the at least one memory module is assigned a last address of the memory when the at least one memory module is decoupled from the at least one bus.

18. The system of claim 17, wherein the at least one memory module is appended to the memory at the last address when the at least one memory module is decoupled from the at least one bus.